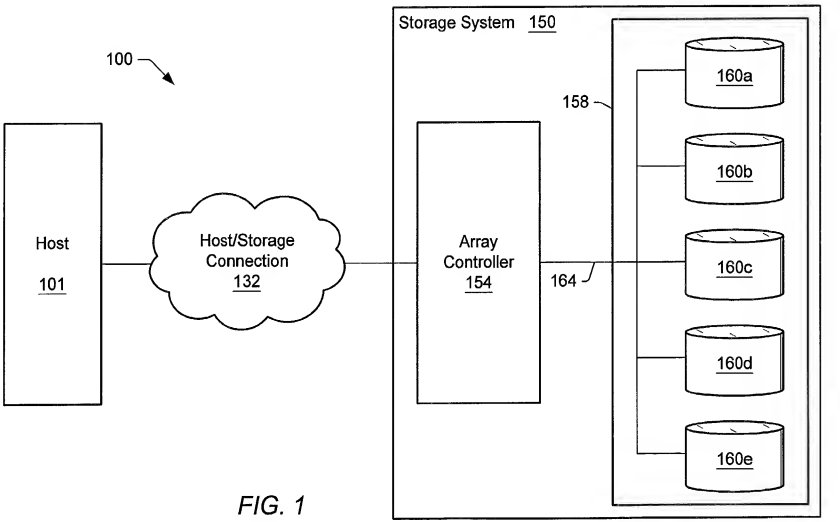
100
Host
101
Host/Storage
Connection
132
Storage System 150
Array
Controller
154
158
164
160a
160b
160c
160d
160e

FIG. 1

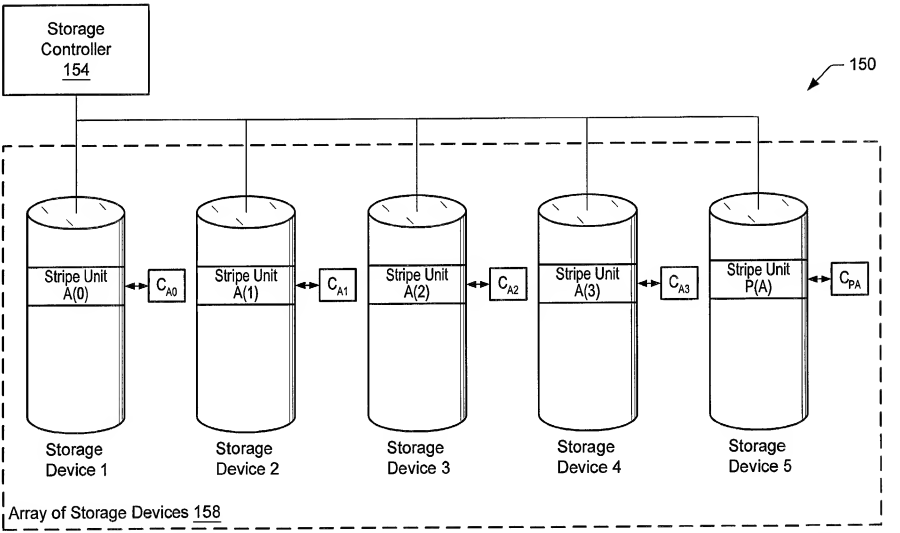
Storage Controller 154
150
Stripe Unit A(0)
C_{A0}
Stripe Unit A(1)
C_{A1}
Stripe Unit A(2)
C_{A2}
Stripe Unit A(3)
C_{A3}
Stripe Unit P(A)
C_{PA}
Storage Device 1
Storage Device 2
Storage Device 3
Storage Device 4
Storage Device 5
Array of Storage Devices 158

FIG. 2

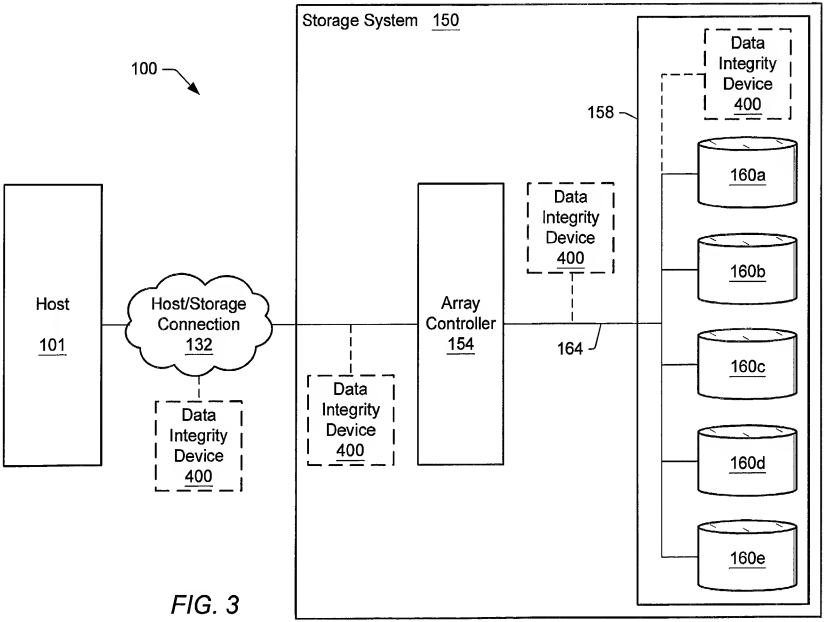
100
Storage System 150
Host
101
Host/Storage
Connection
132
Data
Integrity
Device
400
Data
Integrity
Device
400
Array
Controller
154
Data
Integrity
Device
400
164
158
Data
Integrity
Device
400
160a
160b
160c
160d
160e

FIG. 3

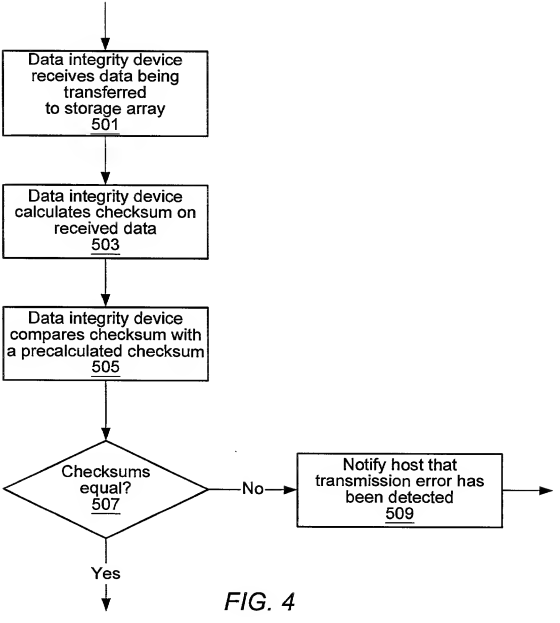
Data integrity device receives data being transferred to storage array
501
Data integrity device calculates checksum on received data
503
Data integrity device compares checksum with a precalculated checksum
505
Checksums equal?
507
No
Notify host that transmission error has been detected
509
Yes

FIG. 4

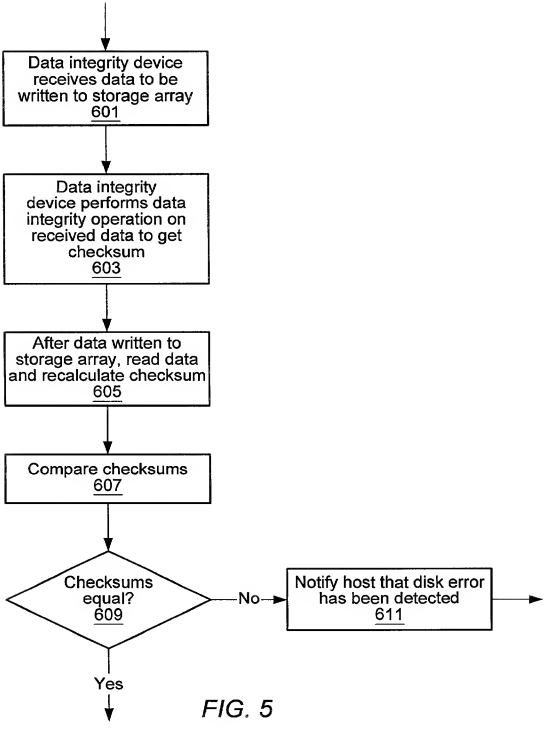
Data integrity device receives data to be written to storage array
601
Data integrity device performs data integrity operation on received data to get checksum
603
After data written to storage array, read data and recalculate checksum
605
Compare checksums
607
Checksums equal?
609
No
Notify host that disk error has been detected
611
Yes

FIG. 5

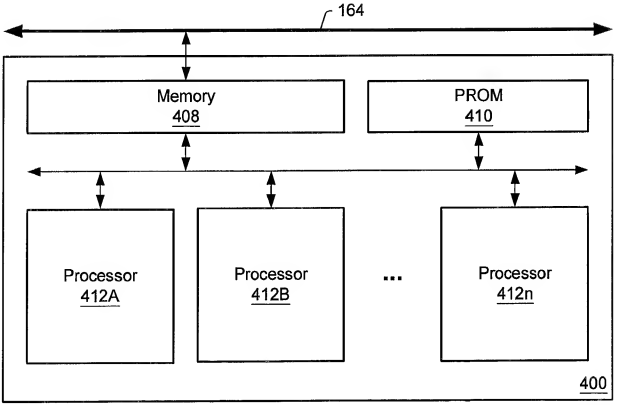
164
Memory
408
PROM
410
Processor
412A
Processor
412B
...
Processor
412n
400

FIG. 6

Data Integrity Device Setting	Description	Effect
N/A	Data integrity device not present in system	Default level of error protection provided by host, array controller, and/or disk drives
0	No processors enabled on data integrity device	Default level of error protection provided by host, array controller, and/or disk drives
1	Single processor enabled in data integrity device	Single data integrity processor performs data integrity operation on data in storage array
2	Two processors enabled in data integrity device	Both processors perform data integrity operation on data and compare results
3	Three processors enabled in data integrity device	Three processors in data integrity device perform data integrity operation on data and vote on results

FIG. 7

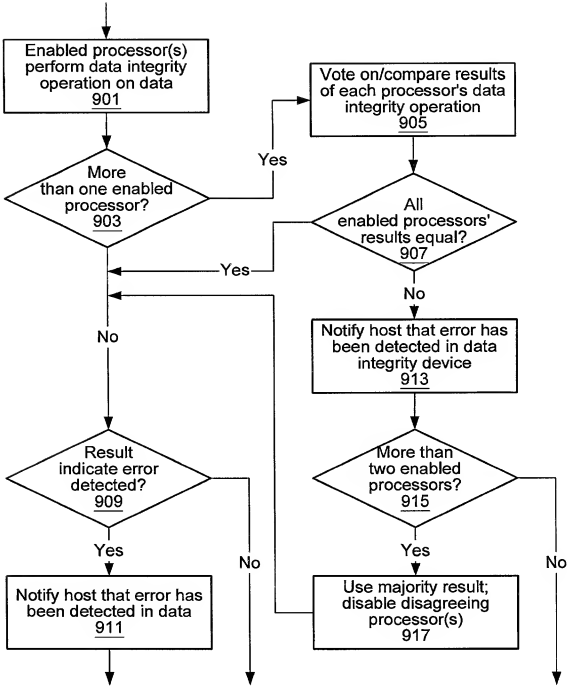
Enabled processor(s) perform data integrity operation on data
901
More than one enabled processor?
903
Yes
No
Vote on/compare results of each processor's data integrity operation
905
All enabled processors' results equal?
907
Yes
No
Notify host that error has been detected in data integrity device
913
Result indicate error detected?
909
Yes
No
Notify host that error has been detected in data
911
More than two enabled processors?
915
Yes
No
Use majority result; disable disagreeing processor(s)
917

FIG. 8

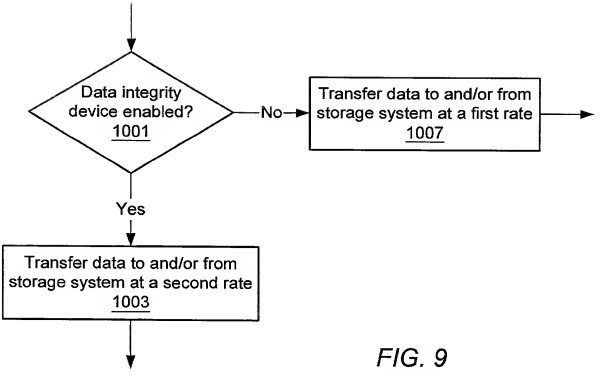

FIG. 9

20070124001

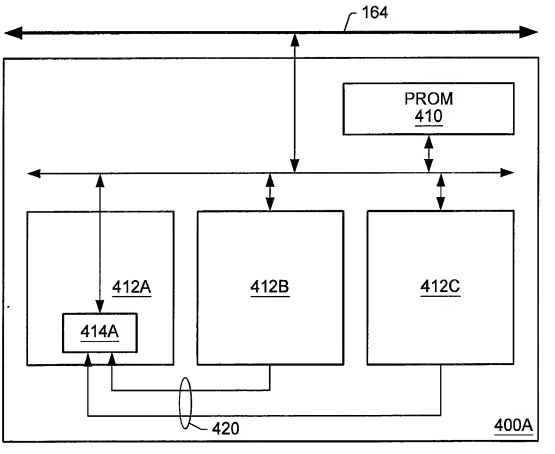

FIG. 10A

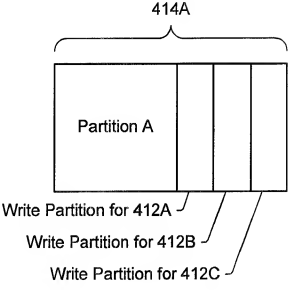

FIG. 10B

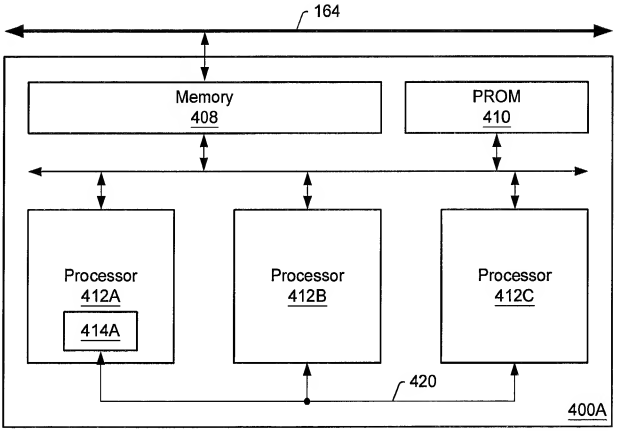
164
Memory
408
PROM
410
Processor
412A
414A
Processor
412B
Processor
412C
420
400A

FIG. 11

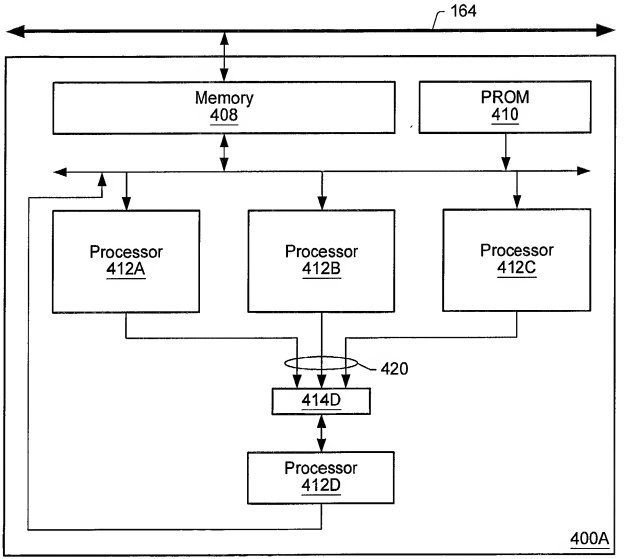
164
Memory
408
PROM
410
Processor
412A
Processor
412B
Processor
412C
420
414D
Processor
412D
400A

FIG. 12

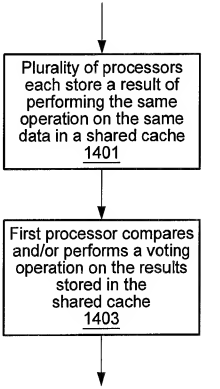
Plurality of processors each store a result of performing the same operation on the same data in a shared cache
1401
First processor compares and/or performs a voting operation on the results stored in the shared cache
1403

FIG. 13